Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 4, with the following amended paragraph:

This application claims benefit of priority under 35 USC § 119 to Japanese Patent Application No. 2000-283337, filed on September 19, 2000, the entire contents of which are incorporated by reference herein.

Please replace the following paragraph beginning at page 2, line 31, with the following amended paragraph:

In FIG. 10, a time difference between when the output UPN of the NAND gate G22 reaches the high level at a falling of the clock signal CLK and when the reference clock signal REFCLK rises to start initialization of the next clock cycle is assumed to be ~~At31~~Δt_{31}. Then, the larger a phase delay time ~~At11~~Δt_{11} of the clock signal CLK with respect to the reference clock signal REFCLK is, the smaller ~~At31~~Δt_{31} becomes.

Please replace the following paragraph beginning at page 3, line 1, with the following amended paragraph:

When frequencies of the reference clock signal REFCLK and clock signal CLK increase, ~~At31~~ Δt_{31} decreases and approaches zero. When ~~At31~~Δt_{31} indicates a negative value, and when the reference clock signal REFCLK rises in the next clock cycle, the output UPN of the NAND gate G22 remains at the low level, the output LC1 of the NAND gate G21 cannot be set to the low level, and normal operation is not realized.

Please replace the following paragraph beginning at page 3, line 8, with the following amended paragraph:

That is, a maximum operation frequency of the conventional phase detector shown in FIG. 10 is defined by the clock frequency at which ~~At11~~Δt_{11} increases and ~~At31~~Δt_{31} becomes zero. In a conventional example, when a phase delay of the clock signal CLK is large with respect to the reference clock signal REFCLK, a timing margin from a point of definition of the signal UPN as

a previous signal of the signal UP until rising of the reference clock signal REFCLK at a start point of the next cycle is reduced. Therefore, the maximum operation frequency is lowered.

Please replace the following paragraph beginning at page 8, line 1, with the following amended paragraph:

In FIG. 7A, the phase detector 10 outputs the high-level UP signal, and the charge pump 11 ~~controls so that~~causes the output voltage ~~goes~~ to go up. On the other hand, in FIG. 7B, the phase detector 10 outputs the high-level DOWN signal, and the charge pump 11 ~~controls so that~~causes the output voltage ~~goes~~ to go down.

Please replace the following paragraph beginning at page 8, line 6, with the following amended paragraph:

~~Since the~~The phase detector 10 of the present embodiment sets the respective outputs of three flip-flops 1 to 3 for controlling generation of the UP and DOWN signals without being directly related to logic of the UP and DOWN signals. Therefore, the UP and DOWN signals can correctly be outputted in accordance with the phase difference between the reference clock signal REFCLK and the clock signal CLK regardless of a magnitude of the phase difference between both signals.